

IN THE CLAIMS

Please amend the claims as follows:

1. (Canceled)
2. (Previously Presented) A multi layer integrated circuit capacitor comprising:
 - a substrate;
 - a first conductive layer located over and contacting the substrate;
 - a first insulator layer located over and contacting the first conductive layer, the first insulator layer not contacting the substrate;
 - a second conductive layer located over the first insulator layer;
 - a second insulator layer located over the second conductive layer;
 - a third conductive layer located over the second insulator layer;
 - a third insulator layer located over the third conductor layer;
 - a plurality of conductive vias downwardly extending through the third insulator layer to provide electrical interconnection to the first, second and third conductive layers; and
 - a plurality of controlled collapse chip connection (C4) lands fabricated on and contacting the third insulator layer and in electrical contact with the plurality of conductive vias.
3. (Original) The multi layer integrated circuit capacitor of claim 2 wherein the C4 lands are fabricated in staggered columns in a plan view.

Claims 4-5. (Canceled)

6. (Previously Presented) A multi layer integrated circuit capacitor comprising:
 - a substrate;
 - a first conductive layer located over and contacting the substrate;

a first insulator layer located over and contacting the first conductive layer, the first insulator layer not contacting the substrate;

a second conductive layer located over the first insulator layer;

a second insulator layer located over the second conductive layer;

a third conductive layer located over the second insulator layer;

a third insulator layer located over the third conductor layer;

a plurality of conductive vias downwardly extending through the third insulator layer to provide electrical interconnection to the first, second and third conductive layers; and
a fourth conductive layer located over the third insulator layer, the fourth conductive layer being patterned to form interconnect lines that selectively connect the plurality of conductive vias.

7. (Previously Presented) A multi layer integrated circuit capacitor comprising:

a substrate;

a first conductive layer located over and contacting the substrate;

a first insulator layer located over and contacting the first conductive layer, the first insulator layer not contacting the substrate;

a second conductive layer located over the first insulator layer;

a second insulator layer located over the second conductive layer;

a third conductive layer located over the second insulator layer;

a third insulator layer located over the third conductor layer; and

a plurality of conductive vias downwardly extending through the third insulator layer to provide electrical interconnection to the first, second and third conductive layers, wherein the second and third conductive layers are fabricated in a plurality of strips, such that a surface area of the second conductive layer is less than a surface area of the first conductive layer and a surface area of the third conductive layer is less than the surface area of the second conductive layer.

8. (Canceled)

9. (Previously Presented) A multi layer integrated circuit capacitor comprising:

a substrate;

a first conductive layer located over and contacting the substrate;

a first insulator layer located over and contacting the first conductive layer, the first insulator layer not contacting the substrate;

a second conductive layer located over the first insulator layer, the second conductive layer being fabricated as a plurality of laterally spaced strips such that a surface area of the second conductive layer is less than a surface area of the first conductive layer;

a second insulator layer located over the second conductive layer;

a third conductive layer located over the second insulator layer, the third conductive layer being fabricated as a plurality of laterally spaced strips such that a surface area of the third conductive layer is less than the surface area of the second conductive layer;

a third insulator layer located over the third conductive layer;

a first plurality of conductive vias downwardly extending through the third insulator layer to provide electrical interconnection to the third conductive layer;

a second plurality of conductive vias downwardly extending through the third insulator layer to provide electrical interconnection to the second conductive layer; and

a third plurality of conductive vias downwardly extending through the third insulator layer to provide electrical interconnection to the first conductive layer.

10. (Previously Presented) The multi layer integrated circuit capacitor of claim 9 further comprising a fourth conductive layer located over the third insulator layer, the fourth conductive layer being patterned to form interconnect lines that selectively connect at least one of the pluralities of conductive vias.

11. (Previously Presented) A multi layer integrated circuit capacitor comprising:

a substrate;

a first conductive layer located over and contacting the substrate;

a first insulator layer located over and contacting the first conductive layer, the first insulator layer not contacting the substrate;

a second conductive layer located over the first insulator layer;

a second insulator layer located over the second conductive layer;
a third conductive layer located over the second insulator layer;
a third insulator layer located over the third conductive layer;
a first plurality of conductive vias downwardly extending through the third insulator layer, the third conductive layer, the second insulator layer, the second conductive layer and the first insulator layer to provide electrical interconnection to the first and third conductive layers;
and

a second plurality of conductive vias downwardly extending through the third insulator layer, the third conductive layer, and the second insulator layer to provide electrical interconnection to the second conductive layer.

12. (Previously Presented) The multi layer integrated circuit capacitor of claim 11 further comprising a fourth conductive layer located over the third insulator layer, the fourth conductive layer being patterned to form interconnect lines that selectively connect at least one of the pluralities of conductive vias.

13. (Previously Presented) The multi layer integrated circuit capacitor of claim 11 wherein at least one of the conductive layers comprise a metal material and wherein at least one of the insulator layers comprise BaSrTiO₃.

14. (Previously Presented) A circuit board assembly comprising:
a circuit board having a pair of supply voltage interconnect lines;
a first integrated circuit die mounted on the circuit board and electrically connected to the supply voltage interconnect lines; and
a second integrated circuit die mounted on the circuit board and electrically connected to the supply voltage interconnect lines, the second integrated circuit die comprising a capacitor having:

a substrate;
a first conductive layer located over and contacting the substrate;

a first insulator layer located over and contacting the first conductive layer, the first insulator layer not contacting the substrate;
a second conductive layer located over the first insulator layer;
a second insulator layer located over the second conductive layer;
a third conductive layer located over the second insulator layer;
a third insulator layer located over the third conductive layer; and
a plurality of conductive vias downwardly extending through the third insulator layer to provide electrical interconnection to the first, second and third conductive layers.

15. (Previously Presented) The circuit board assembly of claim 14 wherein the second integrated circuit die comprises a plurality of controlled collapse chip connection (C4) lands that are electrically connected to the plurality of conductive vias and the supply voltage interconnect lines.

16. (Original) The circuit board assembly of claim 14 wherein the first integrated circuit package is a processor circuit.

17. (Previously Presented) The circuit board assembly of claim 14 wherein at least one of the conductive layers comprise a metal material and wherein at least one of the insulator layers comprise BaSrTiO₃.

18. (Previously Presented) The circuit board assembly of claim 14 further comprising a fourth conductive layer located over the third insulator layer, the fourth conductive layer being patterned to form interconnect lines that selectively connect the plurality of plurality of conductive vias.

19. (Previously Presented) A multi layer integrated circuit capacitor comprising:
a substrate;
a first conductive layer located over and contacting the substrate;

a first insulator layer located over and contacting the first conductive layer, the first insulator layer not contacting the substrate;

a second conductive layer located over the first insulator layer;

a second insulator layer located over the second conductive layer;

a third conductive layer located over the second insulator layer;

a third insulator layer located over the third conductive layer; and

a plurality of conductive vias downwardly extending through the third insulator layer to provide electrical interconnection to the first, second, and third conductive layers, the plurality of conductive vias further extending through the substrate to provide electrical interconnection to both a top surface and a bottom surface of the integrated circuit capacitor.

20. (Previously Presented) The multi layer integrated circuit capacitor of claim 19 further comprising a fourth conductive layer located over the third insulator layer, the fourth conductive layer being patterned to form interconnect lines that selectively connect the plurality of conductive vias.

21. (Previously Presented) The multi layer integrated circuit capacitor of claim 2 wherein each of the conductive layers comprise a metal material and wherein each of the insulator layers comprise BaSrTiO_3 .